Third Semester B.E. Degree Examination, June/July 2018
Analog Electronic Circuits

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1   a.   Derive an expression for E_{Th} , I_B and V_{CE} for voltage divider bias circuit using exact analysis.   **(08 Marks)**

    b.   For the emitter bias network of Fig.Q1(b), determine the following parameters:
         (i) I_B (ii) I_C (iii) V_{CE} (iv) V_C (v) V_E (vi) V_B (vii) V_{BC} **(08 Marks)**
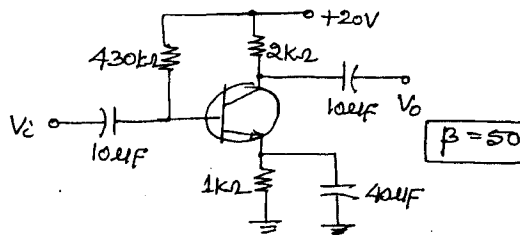

Fig.Q1(b)

OR

2   a.   Derive the expression for stability factor for fixed bias circuit with respect to I_{CO}, V_{BE} and β.   **(10 Marks)**

    b.   With a neat circuit diagram explain the operation of self bias circuit.   **(06 Marks)**

Module-2

3   a.   With the help of r_e equivalent model, derive an equation for input impedance, output impedance and voltage gain for an emitter follower configuration.   **(08 Marks)**

    b.   For the collector feedback configuration having $R_F = 180$ kΩ, $R_C = 2.7$ kΩ, $C_1 = 10$ μF, $C_2 = 10$ μF, $\beta = 200$, $r_0 = \infty$ Ω and $V_{CC} = 9$ volts, determine the following parameters:
         (i) r_e (ii) Z_i (iii) Z_o (iv) A_V **(08 Marks)**

OR

4   a.   High frequency response BJT Amplifier has the following parameters:
         $R_S = 1$ kΩ, $R_1 = 40$ kΩ, $R_2 = 10$ kΩ, $R_E = 2$ kΩ, $R_C = 4$ kΩ, $R_L = 2.2$ kΩ,
         $C_S = 10$ μF, $C_C = 1$ μF, $C_E = 20$ μF, $\beta = 100$, $r_e = 15.76$ Ω, $R_i = 1.32$ kΩ,
         A_{Vmid}(Amplifier) = -90 , $r_0 = \infty$ Ω, $V_{CC} = 20$ V, $C_{be} = 36$ pF, $C_{bc} = 4$ pF, $C_{ce} = 1$ pF,
         $C_{wi} = 6$ pF, $C_{wo} = 8$ pF
         (i) Determine f_{Hi} and f_{Ho} (ii) Determine f_β and f_T **(08 Marks)**

    b.   Derive equations for Miller input capacitance and Miller output capacitance   **(08 Marks)**

Module-3

5   a.   Derive expressions for Z_i and A_i for a Darlington emitter follower circuit.   **(10 Marks)**

    b.   Explain the need of a cascading amplifier? Draw and explain the block diagram of two stage cascade amplifier.   **(06 Marks)**

OR

6 a. List the general characteristics of negative feedback amplifiers. **(04 Marks)**

b. Determine the voltage gain, input impedance and output impedance with feedback for voltage series feedback amplifier having $A = -100$, $R_i = 10$ kΩ, $R_o = 20$ kΩ for feedback of (i) $\beta = -0.1$ and (ii) $\beta = -0.5$. **(06 Marks)**

c. For a current series feedback amplifier, derive an expression for output impedance with feedback. **(06 Marks)**

Module-4

7 a. With a neat circuit and waveforms, explain the operation of a transformer coupled class-A power amplifier. **(08 Marks)**

b. Show that maximum efficiency of class-B push pull power amplifier circuit is 78.54%. **(08 Marks)**

OR

8 a. With a neat circuit diagram and waveform explain the operation of RC phase shift oscillator using BJT. Write the expression for frequency of oscillation. **(08 Marks)**

b. With a neat circuit diagram and waveform, explain the working principle of crystal oscillator operating in series resonant mode. A crystal has the following parameters: $L = 0.334$ H, $C = 0.065$ PF and $R = 5.5$ kΩ. Calculate the resonant frequency. **(08 Marks)**

Module-5

9 a. Derive the expression for A_v, Z_i and Z_o for a JFET common source amplifier with fixed bias configuration. **(08 Marks)**

b. For a self bias JFET circuit, $V_{DD} = +12$V, $R_D = 2.2$ kΩ, $R_G = 1$ mΩ, $R_S = 1$ kΩ $I_{DSS} = 8$mA, $V_P = -4$ volts. Determine the following parameters.
(i) V_{GS} (ii) I_D (iii) V_{DS} (iv) V_S (v) V_G (vi) V_D **(08 Marks)**

OR

10 a. Derive expression for V_{GS}, I_D, V_{DS}, V_D and V_S for a voltage divider bias circuit using FET. **(08 Marks)**

b. With neat sketches, explain the basic operation and characteristics of n-channel depletion type MOSFET. **(08 Marks)**

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